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H.26L intra mode encoder architecture for digital camera application

Tu-Chih Wang , Po-Chih Tseng and Liang-Gee Chen
DSP/IC Lab, National Taiwan University

Abstract— **In this paper, a still image encoder based on H.26L intra mode algorithm is proposed and implemented in a FPGA prototype board. H.26L[1] is proposed by ITU-T to provide high compression efficiency for very low bit rate communication. Intra mode in H.26L (H.26Li) uses high level spatial prediction and provides 2 db PSNR gain more than JPEG standard. It is suitable for still image camera application and can be further extended into video camera application.**

I. Introduction

In a digital camera system, image compression is very important due to limited storage space. In today's market, JPEG is the most popular compression format for digital camera application. But the compression ratio of JPEG is low in today's view point. JPEG group has announced JPEG2000[4] for the next generation of still image compression. The target of JPEG2000 is mainly low bitrate application. And the performance of JPEG2000 on medium to high bitrate is almost the same as JPEG. For digital camera application, target bitrate is often set at medium to high to get better image quality. In this range, JPEG2000 is not a good candidate for digital camera application. Moreover, JPEG2000 is based on wavelet transform, which requires whole frame buffer to process. The frame buffer is proportional to image resolution. So if the resolution of camera grows, the frame buffer would be even larger. Thus, the complexity of JPEG2000 encoder is much higher and hardly to cost down. H.26L is mainly designed for very low bitrate video communication. The algorithm of H.26Li is block based and using spatial prediction. Comparing to JPEG, H.26Li provides better performance on medium to high bitrate. And the hardware cost is not as much as JPEG2000. The comparison between these standards are given below.

II. H.26Li algorithm

H.26Li uses a block transform algorithm. The picture is decomposed into 16 × 16 macroblock. Each macroblock is formed by 16 4 × 4 block. The block size of H.26Li is different from JPEG for less block artifacts. 8 × 8 2D DCT is replaced by 4 × 4 2D DCT for luminace and 2 × 2 2D transform for chrominace. The coding gain of H.26Li comes from spatial prediction. There are seven 4 × 4 prediction modes and four 16 × 16 prediction modes to eliminated spatial redundancy.4 × 4 prediction modes are used to deal with detailed texture block, while 16 × 16 prediction mode could provide higher compression gain in large flatten area. The remain residual is then coded using 4 × 4 DCT , quantization, scan, and VLC process. The coding efficiency of JPEG and H.26Li is shown in Fig.1.The algorithm flow in H.26Li is shown in Fig.2. The test image is a 768 × 512 image from [3]. Fig.1 shows only PSNR of luminance which is most sensitive to human eyes. PSNR of chrominace for H.26Li is also higher than the one for JPEG in all compression ratio.

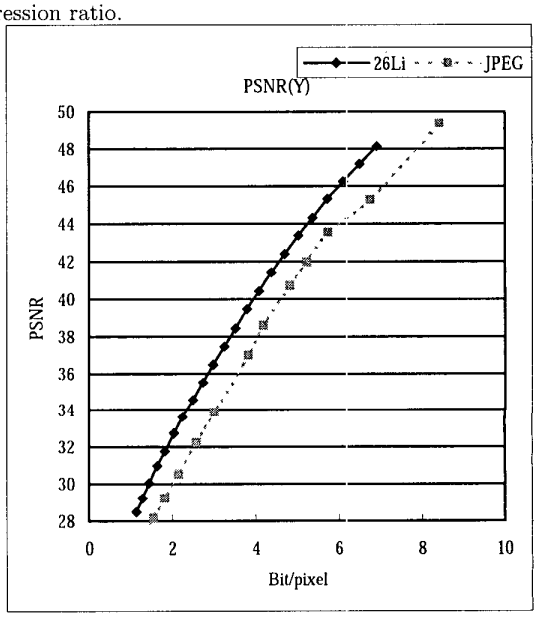

Fig. 1. Performance comparison of JPEG and H.26Li

III. H.26Li encoder architecture

Fig. 3 is the architecture of H.26Li encoder. Image is first fed into spatial prediction engine to find out which mode is the best among these eleven spatial prediction modes. Codewords described mode information are sent to mode table. Two block prediction modes produce one VLC codeword. Prediction macroblock is then subtracted from original image and then sent into transform unit, quantization unit, scan unit, and VLC unit. The architecture is almost the same as JPEG except for spatial prediction and mode selection. The transform unit is reduced to 4 × 4 DCT transform and 2 × 2 transform so that the hardware cost for these units could be largely reduced. The VLC

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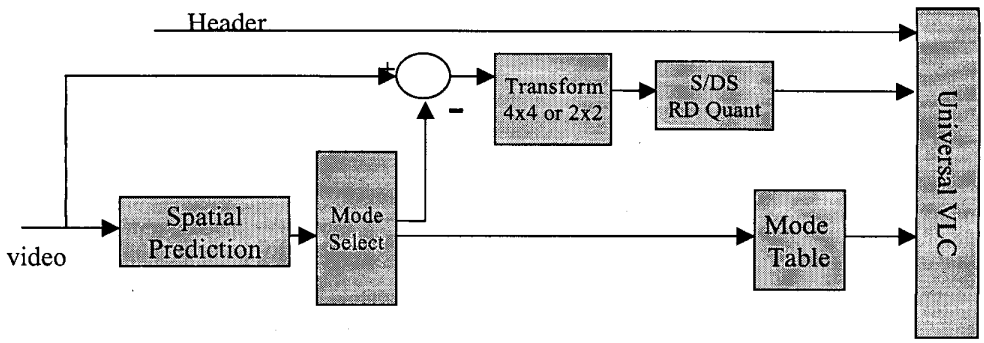

Fig. 2. H.26Li encoder block diagram

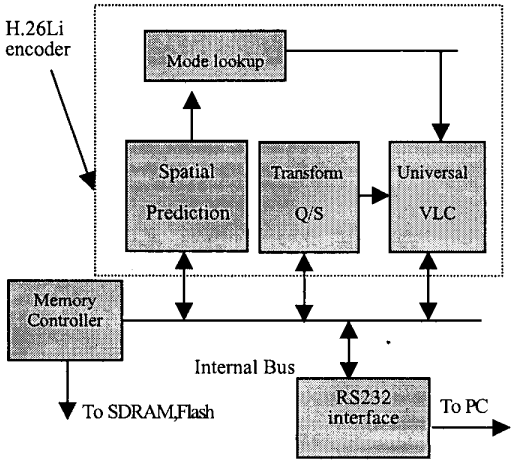

Fig. 3. H.26Li encoder system architecture

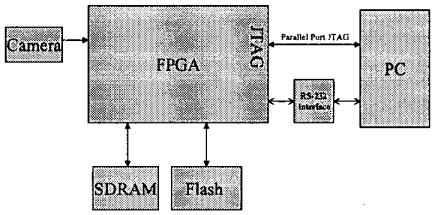

Fig. 4. Prototype system diagram

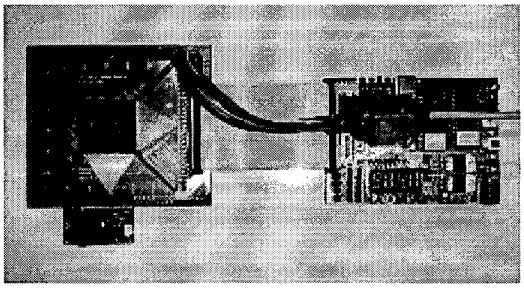

Fig. 5. Prototype board photo

used in H.26Li only has one pattern and is more regular than JPEG standard.

IV. Prototype Environment

The encoder architecture is mapped into a Xilinx Virtex 800 FPGA prototype board. The capacity of Virtex 800 is about 800k gate count and is large enough for our encoder. The block diagram of the prototype system and it's photo are shown in Fig.4 and Fig.5. We use a single chip APS camera from OmniVision to provide input image. Also, a RS-232 UART port is synthesized in FPGA connected with MAX232 to provide connection to PC. FPGA initialization could use parallel port on PC to download design in design phase and use EEPROM when the design is finished. The SDRAM and flash interfaces are used for temporary data and compression bitstream. We also use these memories to provide test data in individual function when we finish each unit.

V. Conclusions

An encoder architecture suitable for still image application is presented in this paper. Using H.26L intra mode coding algorithm, image quality could be improved at the same compression ratio. This architecture could also be extended to encode video.

References

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